Remarks

Applicant respectfully requests that this Amendment After Final Action be admitted under 37 C.F.R. § 1.116.

Applicant submits that this Amendment presents claims in better form for consideration on appeal. Furthermore, applicant believes that consideration of this Amendment could lead to favorable action that would remove one or more issues for appeal.

Claims 1, 16 and 23 have been amended. No claims have been canceled. Therefore, claims 1, 2, 4-8, 10-17, and 19-30 are now presented for examination.

Claims 23-30 stand rejected under 35 U.S.C. §102(b) as being anticipated by Levy et al. (U.S. Patent No. 6,092,175). Applicant submits that the present claims are patentable over Levy.

Levy discloses a method and organization for implementing the registers required in a computer system supporting multithreading and dynamic out-of-order execution. Multithreaded computer systems are those in which the processor supports multiple contexts (threads), and either rapid context switching from thread to thread or scheduling of instructions from different threads within a single cycle. An important component of processors for such systems is the register file; the processor needs a large register file or resource to provide the registers used for the threads. One form of the invention maintains a set of private architecturally specified registers, and a set of private renaming register for each different thread. In the other three embodiments, sharing of renaming registers between different threads is permitted, to enable a reduction in the total number of registers required. One of these three embodiments enables any of the architecturally

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specified registers that are private to a thread but are not in use, to be employed as renaming registers. Another of the embodiments treats all registers as sharable and enables any register from the register file or resource to be used as a renaming register for any thread.

Claim 23 of the present application recites allocating a first set of physical registers to first logical registers associated, allocating a second set of physical registers to second logical registers and dividing a freelist of registers equally for a first thread and a second thread. Applicant submits that Levy does not disclose such a feature. Therefore, claim 23 and its dependent claims are patentable over Levy.

Claims 1, 2, 4-8, 10-17, and 19-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy et al. (U.S. Patent No. 6,092,175) in view of Leibholz (U.S. Patent No. 6,954,846). Applicant submits that the present claims are patentable over Levy even in view of Leibholz.

Leibholz discloses a microprocessor that is capable of executing in either a multi-thread mode or a single thread mode. In the multi-thread mode, each active thread may have an associated register file which the thread may access. In the single thread mode, a single thread is active and the thread has access to all of the available register files. In one embodiment of the present invention, two threads may simultaneously execute and there are two register files. In the single thread mode, the single active thread may have access to both of the register files. See Leibholz at col. 1, ll. 55-67.

Claim 1 of the present application recites entries in a list of physical registers within the physical register file that are not allocated to a logical register being partitioned such that a first portion of the entries are allocated to a first thread and a

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second portion of the entries are allocated to a second thread, wherein the second portion is equal to the first portion.

Applicant submits that that neither Levy nor Leibholz disclose or suggest equally partitioning entries in a list of physical registers within the physical register file that are not allocated to a logical register such that a first portion of the entries are allocated to a first thread and a second portion of the entries are allocated to a second thread. The Final Office Action asserts that Leibholz discloses such a feature. See Final Office Action at Page 6, paragraph 13.

Applicant respectfully disagrees with such an assertion. Leibholz discloses an embodiment where two threads may simultaneously execute and there are two register files, and in the single thread mode, the single active thread may have access to both of the register files. See Leibholz at col. 1, ll. 63-67. Nonetheless, applicant submits that employing two separate register files while operating in a multiple thread mode is not equivalent to equally dividing a list of physical registers within a single physical register file that are not allocated to a logical register.

Because neither Levy nor Leibholz disclose or suggest equally partitioning entries in a list of physical registers within the physical register file that are not allocated to a logical register such that a first portion of the entries are allocated to a first thread and a second portion of the entries are allocated to a second thread, any combination of Levy and Leibholz would also fail to disclose or suggest such a feature. Thus, claim 1 and its dependent claims are patentable over Levy in view of Leibholz.

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Independent claims 8 and 16 include limitations similar to those recited in claim 1. Therefore claims 8 and 16, and their respective dependent claims, are also patentable over Levy in view of Leibholz for reasons similar to those recited in claim 1.

Applicant respectfully submits that the rejections have been overcome, and that the claims are in condition for allowance. Accordingly, applicant respectfully requests the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,
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Date: February 27, 2008   _____

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